

Applicant: Fernando Gonzalez, et al.

Confirmation No.: 7257

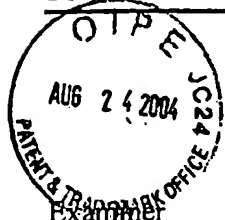
Serial No.: 10/804,477

Att'y Docket No.: 11675.22.2.1.3.1

Filing Date: March 19, 2004

Group: 2812

For: METHOD OF MAKING VERTICAL DIODE STRUCTURES

INFORMATION DISCLOSURE CITATIONS MADE BY APPLICANTU.S. Patent Documents

<u>Initial*</u>	<u>Document Number</u>	<u>Issue Date</u>	<u>Name</u>
<u>ME</u> 1	3,615,929	10/26/1971	Portnoy et al.
<u>ME</u> 2	3,664,896	05/23/1972	Duncan
<u>ME</u> 3	3,777,364	12/11/1973	Schinella et al.
<u>ME</u> 4	3,914,137	10/21/1975	Huffman et al.
<u>ME</u> 5	3,928,095	12/23/1975	Harigaya et al.
<u>ME</u> 6	3,990,099	11/02/1976	Duigon et al.
<u>ME</u> 7	4,404,737	09/20/1983	Kanzaki et al.
<u>ME</u> 8	4,414,737	11/14/1983	Menjo et al.
<u>ME</u> 9	4,530,149	07/23/1985	Jastrzebski et al.
<u>ME</u> 10	4,589,193	05/20/1986	Goth et al.
<u>ME</u> 11	4,619,887	10/28/1986	Hooper et al.
<u>ME</u> 12	4,666,556	05/19/1987	Fulton et al.
<u>ME</u> 13	4,742,014	05/03/1988	Hooper et al.
<u>ME</u> 14	4,784,969	11/15/1988	Nitayama
<u>ME</u> 15	4,922,319	05/1990	Fukushima
<u>ME</u> 16	5,022,742	06/1991	Hains
<u>ME</u> 17	5,070,383	12/1991	Sinar et al.

CLASS
SUB
CLASS

Examiner:

Michelle Bottrada

Date Considered:

10/14/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant: Fernando Gonzalez, et al.

Confirmation No.: 7257

Serial No.: 10/804,477

Att'y Docket No.: 11675.22.2.1.3.1

Filing Date: March 19, 2004

Group: 2812

For: METHOD OF MAKING VERTICAL DIODE STRUCTURES

<u>ME</u> 18	5,162,245	11/10/1992	Favreau
<u>ME</u> 19	5,163,178	11/10/1992	Gomi et al.
<u>ME</u> 20	5,213,989	05/25/1993	Fitch et al.
<u>ME</u> 21	5,231,038	07/27/1993	Yamaguchi et al.
<u>ME</u> 22	5,236,851	08/17/1993	Kameyama et al.
<u>ME</u> 23	5,236,852	08/17/1993	Cherniawski et al.
<u>ME</u> 24	5,268,316	12/1993	Robinson et al.
<u>ME</u> 25	5,272,097	12/1993	Shiota
<u>ME</u> 26	5,355,301	10/1994	Saito et al.
<u>ME</u> 27	5,366,908	11/22/1994	Pelella
<u>ME</u> 28	5,407,851	04/1995	Roesner
<u>ME</u> 29	5,420,053	05/30/1995	Miyazaki
<u>ME</u> 30	5,441,907	08/1995	Sung et al.
<u>ME</u> 31	5,464,782	11/07/1995	Koh
<u>ME</u> 32	5,494,848	02/27/1996	Chin
<u>ME</u> 33	5,567,644	10/1996	Rolfson et al.
<u>ME</u> 34	5,589,418	12/31/1996	Kalnitsky
<u>ME</u> 35	5,508,224	04/16/1996	Jang
<u>ME</u> 36	5,510,287	04/23/1996	Chen et al.
<u>ME</u> 37	5,529,943	06/25/1996	Hong et al.

Class
210
C1054

Examiner:

Michelle Estrada

Date Considered:

10/14/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant: Fernando Gonzalez, et al.
 Serial No.: 10/804,477
 Filing Date: March 19, 2004
 For: METHOD OF MAKING VERTICAL DIODE STRUCTURES

Confirmation No.: 7257
 Att'y Docket No.: 11675.22.2.1.3.1
 Group: 2812

Class 3825 C1025

<i>me</i> 38	5,550,075	08/27/1996	Hsu et al.
<i>me</i> 39	5,597,741	01/28/1997	Sakamoto et al.
<i>me</i> 40	5,616,946	04/01/1997	Hsu, et al.
<i>me</i> 41	5,652,182	07/29/1997	Cleeves
<i>me</i> 42	5,670,417	09/23/1997	Lambson et al.
<i>me</i> 43	5,683,939	11/04/1997	Schranz et al.
<i>me</i> 44	5,714,768	02/03/1998	Ovshinsky et al.
<i>me</i> 45	5,739,563	04/14/1998	Kawakubo et al.
<i>me</i> 46	5,773,346	06/30/1998	Manning
<i>me</i> 47	5,780,343	07/14/1998	Bashir
<i>me</i> 48	5,804,476	09/08/1998	Jang
<i>me</i> 49	5,856,214	01/05/1999	Yu
<i>me</i> 50	5,998,244	12/07/1999	Wolstenholme et al.
<i>me</i> 51	6,057,195	05/02/2000	Wu
<i>me</i> 52	6,420,725 B1	07/16/2002	Harshfield

Foreign Patent Documents

Examiner Initial*	Document Number	Publication Date	Country or Patent Office	Translation
<i>me</i> 53	01112780 A	05/01/1989	Japan	Abstract

Examiner: *Michelle Estrada* Date Considered: *10/14/04*

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant: Fernando Gonzalez, et al.

Confirmation No.: 7257

Serial No.: 10/804,477

Att'y Docket No.: 11675.22.2.1.3.1

Filing Date: March 19, 2004

Group: 2812

For: METHOD OF MAKING VERTICAL DIODE STRUCTURES

34	01196863 A	08/1989	Japan	
55	03280582 A	12/11/1991	Japan	Abstract
56	DE 10005774 A1	08/23/2001	Germany	Abstract

Other Documents

(including author, title, pertinent pages, etc.)

Examiner

Initial*

37 Wolf, Silicon Processing for the VLSI Era, Vol. 1, Process Technology, pages 136-139, Lattice Press

References Cited by Applicants

While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

Each citation initialed by the Examiner will be printed on the issued patent in the same manner as references cited by the Examiner on Form PTO-892.

The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

W:\11675\22.2.1.3.1\GPM0000000266V001.doc

Examiner:

Michelle Estrada

Date Considered:

10/14/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.